Fully Depleted CIS Pixel Using Reverse Substrate Bias without Undesirable Leakage Currents

Swaraj Bandhu Mahato[1, †], Jean-Luc Bacq[1], Pierre Boulenc[1,2], Yun-Tzu Chang[1], Bert van Lijnschoten[1], Antonia Malainou[1], Celso Cavaco[1]
[1] imec, Kapeldreef 75, B-3001 Leuven, Belgium
[2]Now with Gpixel NV, Antwerp, Belgium
[†]Email: Swaraj.Mahato@imec.be

Abstract— Earlier, IMEC has demonstrated a fully depleted CIS pixel device with a sufficiently large reverse substrate bias or back bias. In this paper, we report an updated device structure that circumvents the die leakage and punch-through in the peripheral circuit area and is used in an ultra-high speed CMOS image sensor. The updated device structure is designed and studied through TCAD simulations and validated through leakage measurement and pixel characterization.

INTRODUCTION

Fully depleted CMOS image sensors are attractive for ultra-high-speed imaging [1-2] along with many other advanced applications such as soft X-ray detection, time-of-flight imaging etc. [3-8]. IMEC has developed a CMOS compatible platform in 130nm monolithic CIS process for fully depleted image sensor [9]. Pixel test array built with fully depleted pixels in IMEC's technology has already demonstrated a working device with 30µm epi thickness. Thick sensitive semiconductor volume is depleted by applying sufficient reverse bias across the substrate, so that field-free regions are eliminated, and the strong electric field drives the fast photocarrier transport to the sense node. During further development of a complete imager using such devices with high back-bias, the sensor had suffered from high leakage over the back contact and punch-through current between deep pWells and backside p+ region. In this paper, we report an updated device structure that circumvents the die leakage and punch-through in the peripheral circuit area and is used in an ultra-high speed CMOS image sensor.

PIXEL TECHNOLOGY AND LEAKAGE

A fully depleted substrate pixel technology was specifically developed for a high-speed image sensor by employing strong electric field for fast photocarrier transport while minimizing lateral crosstalk [10]. A cross-section of the technology is depicted in Fig.1. Fully depleted substrate is achieved by dedicated doping profile design as well as by applying a large reverse substrate bias or back bias having a sufficiently large voltage difference between the floating diffusion (FD) junction and a backside contact. The magnitude of the back bias depends on the resistivity and the thickness of the substrate and far exceeds other operating voltages in the system [5]. The in-pixel readout circuit is embedded inside a dedicated pWell and peripheral readout circuits in standard 0.13µm CMOS technology are insulated from the epitaxial layer by means of a deep pWell implant. The pixel area is shielded from the CMOS area by an n-guard ring to avoid transport of carriers generated below the CMOS area towards the pixel area.

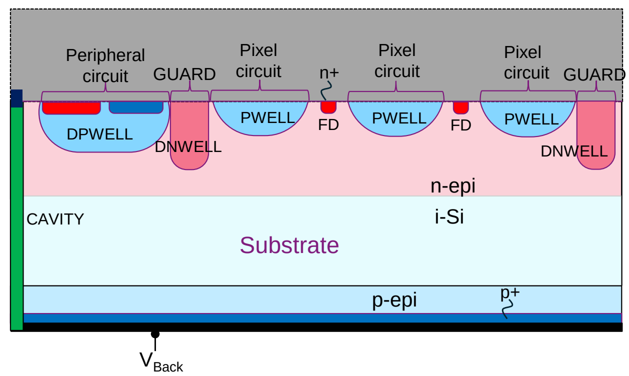


Fig 1:Device cross-sectional view recreated from [2].

Applying a high back bias to conventional CMOS image sensor technology will result in resistive leakage current over the epitaxial layer and respective back contact. As said earlier, when we were developing a complete imager using such devices with high back-bias, the sensor had suffered from high leakage over the back contact and punch-through current between deep pWells and backside p+ region. Those were not fully anticipated in the previous test vehicle.

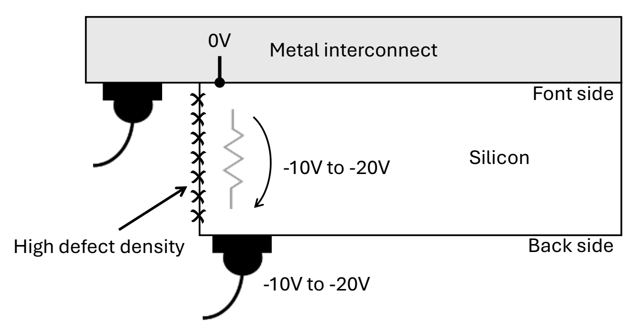


Fig 2:Schematic diagram of the resistive leakage from back side.

The root-cause being the excessive parasitic leakage current in the peripheral areas is accounted as perimeter leakage. During BSI processing, cavities are etched into silicon to be able to interface the metal interconnects and allow for back side bonding. Usually, this interface can have high defect density which implies that once the high back bias is applied over the silicon a resistive current is pulled from the backside to the front side (Fig.2), named as perimeter leakage. Additionally, as back bias increases, holes from the deep pWell of the CMOS circuit area can overcome the built-in potential barrier, which causes the observed punch-through current.

PIXEL DESIGN TO MITIGATE PERIMETER LEAKAGE AND PUNCH-THROUGH

To mitigate perimeter leakage, we implemented an additional substrate-biased outer pWell on the front side and an extra n-guard ring surrounding the peripheral circuit area such that the required voltage drop is not dealt with along the highly defective interface of the cavity but along the high-quality front-side surface developed for high quality CMOS transistors as depicted in Fig.3.

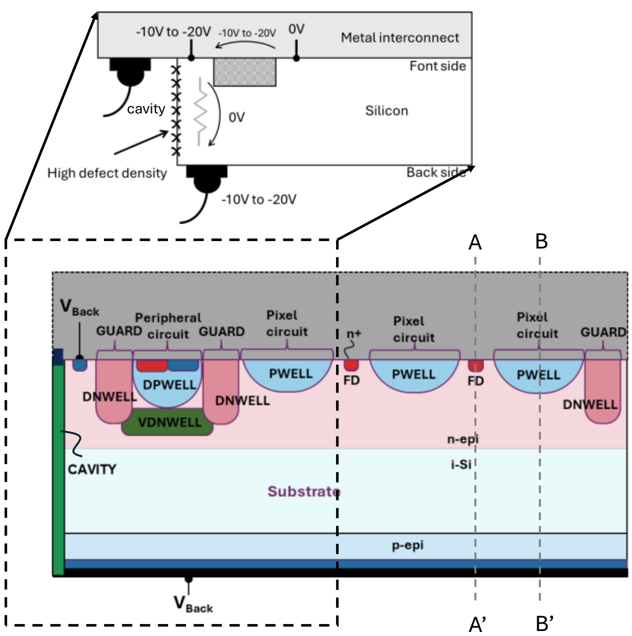


Fig 3: Proposed device cross-sectional view and schematic of the proposed solution for resistive leakage.

To eliminate the hole punch-through from the deep pWell of the CMOS peripheral circuit, we implemented a very deep nWell under the peripheral circuit area which is connected to the two n-guard ring as depicted also in the Fig.3. After securing the hole punch-through from the deep pWell of the CMOS peripheral circuit, device needs to be farther optimized for high back bias to address the trade-off between leakage and the possible punch-through to the in-pixel readout circuit embedded inside a dedicated pWell, which is shielded by the n-epi through a built-in potential barrier. So the trade-off is to be as close as possible to the punch-through voltage (to get complete depletion) but still having a low leakage caused by the lowering of the barrier.

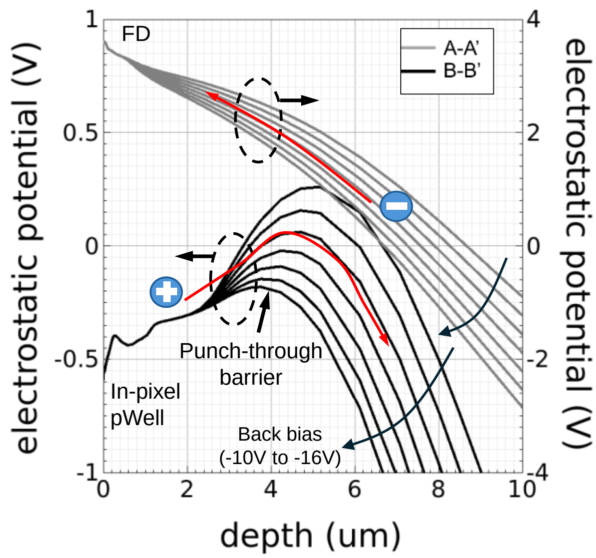


Fig 4: Simulated electrostatic potential profiles through cuts A-A' and B-B' of Fig.3.

For design optimization and analysis, we made a TCAD model of the updated device to do relevant simulations. Electrostatic potential profiles through pWell – that embeds the pixel circuit –, and epitaxial layer (B-B') as well as through FD and epitaxial layer (A-A') for different back bias (-10V to -16V)

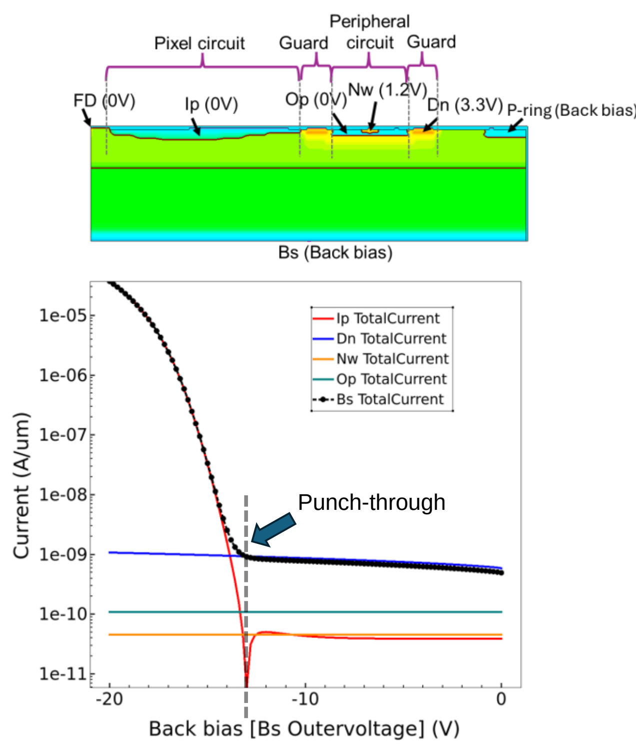


Fig 5: Simulated currents for different substrate bias (TCAD). Here, Ip = inner pWell that embeds the pixel circuit, Dn = deep n-guard rings surrounding the peripheral circuit, Nw = CMOS nWell inside peripheral circuit, Op = outer pWell that embeds the peripheral circuit, and Bs = back side of the substrate.

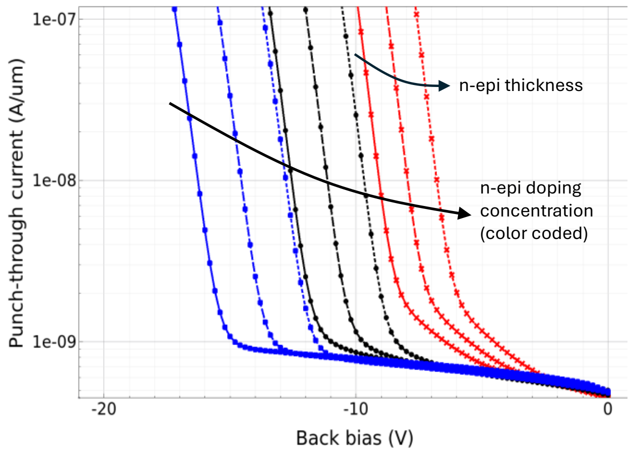


Fig 6: Puch-through current for different n-epi thickness and doping concentrations (TCAD). 3 sets of n-epi doping concentrations are color coded here. For each set, 3 different n-epi thicknesses are simulated. Here arrow indicates the decrement in the respective parameter.

are depicted in Fig. 4. From upper subfigure, we can see as the built-in potential barrier is graded towards the FD, carriers will swiftly migrate to the FD as well. The lower sub-figure illustrates that majority carriers of the pWell can overcome the built-in potential barrier more likely if the back bias is increased. Suppression of any punch-through current from backside to the in-pixel readout circuit embedded inside a dedicated pWell is addressed by built-in potential barrier optimization. To do that, we conduct electrostatic simulation of the device and extract different currents for varying back bias. Fig.5 illustrates simulated current of the device (TCAD model) depicted in the upper subfigure for different back bias. At around -13V back bias, punch-through is started in the pWell that embeds the pixel circuit. This result has been reached by optimizing the n-epi thickness and doping concentration of the device as depicted in Fig.6. Three sets of different n-epi doping concentrations are simulated where each set contains 3 different n-epi thicknesses for same doping concentration. Punch-

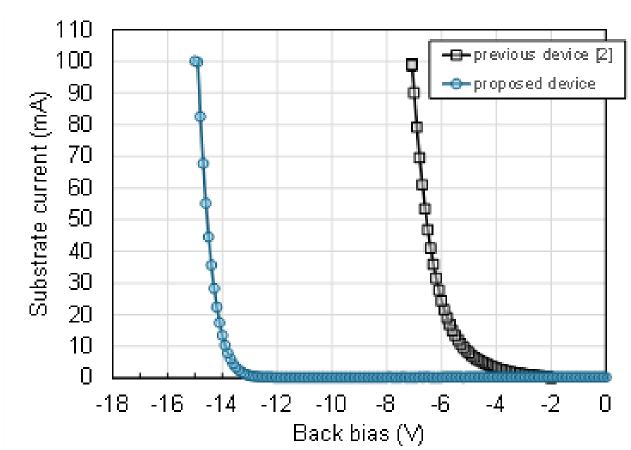


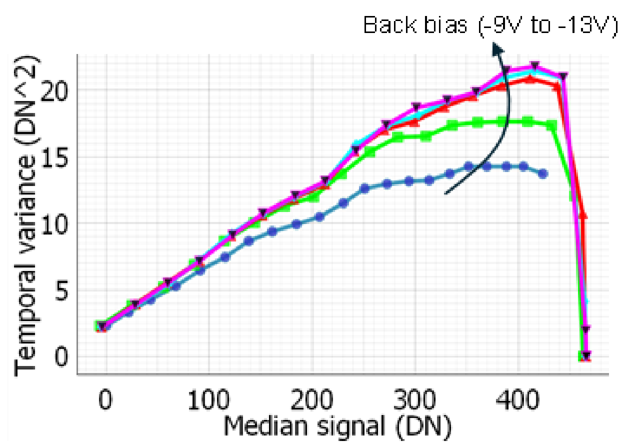
Fig 7: Substrate current measurement to compare previous and the proposed device with mitigations.

through voltage increases as n-epi thickness as well as doping concentration increases. A trade-off between punch-through current and leakage current has to be made to achieve required back bias to reach desire charge transfer speed.

Measurement Results

Measurement is performed to validate the proposed solution for the high leakage over the back contact. In Fig. 7, measured full chip substrate current shows that the previously demonstrated device with high leakage restricts the required high back bias, whereas after the mitigation in newly proposed device, >12V of back bias can be applied as it designed for.

Fig. 8 shows PTC plots of the sensor with different back bias. At lower back bias than the designed one (~ -13V), significant non-linearity at higher signal level can be observed which is getting better with higher back bias. This shows that the temporal variance is saturating at higher signal level due to signal sharing across the pixel array and indicates that the pixel may not be fully depleted at lower back bias. The results of



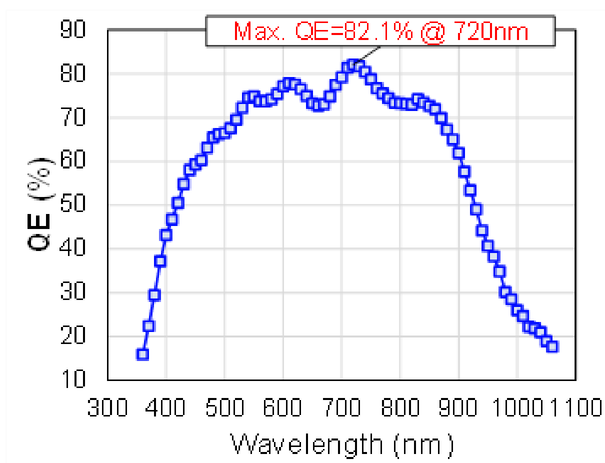


Fig 9: Measured Quantum Efficiency (QE) curve for different wavelengths.

quantum efficiency (QE) measurement using monochromatic light source are plotted in Fig. 9. Using BSI post-processing, the sensor evidently achieves high QE.

CONCLUSION

Problem of high leakage over the back contact and punch-through current between deep pWells and backside p+ region are identified in our previous fully depleted CIS pixel device. In this paper, we proposed an updated pixel device to mitigate these problems. Proposed device structure is designed and optimized through TCAD simulations, and the mitigation approach is validated through leakage measurement and pixel characterization.

REFERENCES

[1] V. T. S. Dao et al., “Toward 10 Gfps: Factors Limiting the Frame Rate of the BSI MCG Image Sensor,” IISW 2015, June 2015.

[2] T. Resetar et al., “Development of Gated Pinned Avalanche Photodiode Pixels for High-Speed Low-Light Imaging,” Sensors 2016, 16, 1294, Aug. 2016.

[3] M. Havranek et al., “DMAPS: a fully depleted monolithic active pixel sensor – analog performance characterization,” 2015 JINST 10 P02013, Feb. 2015.

[4] P. Rymaszewski et al., “Prototype Active Silicon Sensor in 150 nm HR-CMOS Technology for ATLAS Inner Detector Upgrade,” 2016 JINST 11 C02045, Feb. 2016.

[5] K. D. Stefanov, A. S. Clarke and A. D. Holland, "Fully Depleted Pinned Photodiode CMOS Image Sensor With Reverse Substrate Bias," in IEEE Electron Device Letters, vol. 38, no. 1, pp. 64-66, Jan. 2017.

[6] Lucio Pancheri st al., “A 110nm CMOS process with fully depleted high resistivity substrate for NIR, X-ray and charged particle imaging”, in IISW, 2019.

[7] A. Payne et al., “A 512x424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130 MHz and 2GS/s ADC,” ISSCC 2014, pp. 134-136, Feb. 2014.

[8] A. Clarke et al., “Fully depleted, thick, monolithic CMOS pixels with high quantum efficiency,” 2015 JINST 10 T04005, April 2015.

[9] Imec’s white paper about “monolithic microsystems”, page 12, URL: https://www.imec-int.com/en/what-we-offer/design-and-foundry-services/white-paper-monolithic-microsystems

[10] A. Süss, L. Wu, J.-L. Bacq, A. Spagnolo, P. Coppejans, V. Motsnyi, L. Haspeslagh, J. Borremans and M. Rosmeulen, "A Fully Depleted 52 µm GS CIS Pixel with 6 ns Charge Transfer, 7 e-rms Read Noise, 80 µV/e- CG and >80 % VIS-QE," in IISW, 2017.